

**Amendments to the Claims:**

This listing of the claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims**

1. (Currently amended) A method of forming a capacitor on an integrated circuit comprising:
  - forming a lower electrode of the capacitor on an integrated circuit substrate;
  - forming a nitride protection layer on the lower electrode at a temperature below a minimum temperature associated with a phase change of the lower electrode;
  - forming a dielectric layer on the protection layer, wherein the protection layer is configured to limit oxidation of the lower electrode during forming of the dielectric layer; and
  - forming an upper electrode of the capacitor on the dielectric layer.
2. (Original) The method of Claim 1 wherein the first lower electrode comprises an amorphous silicon layer, a polycrystalline silicon layer and/or a composite layer thereof.
3. (Currently amended) The method of Claim 1 wherein the nitride protection layer comprises a silicon nitride layer.
4. (Original) The method of Claim 3 wherein forming the protection layer comprises forming the nitride layer at a temperature of about 600°C or less using a plasma nitration process.
5. (Original) The method of Claim 3 wherein forming the protection layer comprises forming the nitride layer at a temperature of about 600°C or less using a chemical vapor deposition process and/or an atomic layer deposition process.

6. (Original) The method of Claim 3 wherein forming the protection layer comprises forming the nitride layer at a temperature of about 600°C or less using a microwave-type deposition process.
7. (Original) The method of Claim 1 wherein the dielectric layer comprises a metal oxide layer.
8. (Original) The method of Claim 7 wherein the metal oxide layer comprises a TiO<sub>2</sub> layer, an Al<sub>2</sub>O<sub>3</sub> layer, an Y<sub>2</sub>O<sub>3</sub> layer, a ZrO<sub>2</sub> layer, an HfO<sub>2</sub> layer, a BaTiO<sub>3</sub> layer, an SrTiO<sub>3</sub> layer and/or a composite layer thereof.
9. (Original) The method of Claim 7 wherein forming the dielectric layer comprises forming the metal oxide layer at a temperature of about 600°C or less using a chemical vapor deposition process and/or an atomic layer deposition process.
10. (Original) The method of Claim 1 wherein the protection layer comprises a silicon nitride layer.
11. (Original) The method of Claim 1 wherein the upper electrode comprises an amorphous silicon layer, a polycrystalline silicon layer, an Ru layer, a Pt layer, an Ir layer, a TiN layer, a TaN layer, a WN layer and/or a composite layer thereof.
12. (Original) The method of Claim 1 wherein the lower electrode comprises a cylindrical lower electrode and wherein forming a lower electrode comprises:
  - forming a lower structure on the integrated circuit substrate;
  - forming an insulation layer pattern having a contact hole on the lower structure;
  - forming a conductive plug in the contact hole;
  - forming an oxide layer patterned to have a cylindrical shape on the insulation layer

pattern and the plug;

forming a conductive layer for the lower electrode on the oxide layer; and  
removing the oxide layer to form the cylindrical lower electrode.

13. (Original) The method of Claim 12 wherein forming the protection layer comprises forming the protection layer on the cylindrical lower electrode.

14. (Currently amended) A method of forming a capacitor comprising:  
forming a first conductive layer on a substrate;  
forming a reaction-preventing nitride layer on the first conductive layer to prevent an oxidation at a temperature of not generating a phase change of the first conductive layer;  
forming a dielectric layer on the reaction preventing nitride layer; and  
forming a second conductive layer on the dielectric layer.

15. (Original) The method of Claim 14 wherein the first conductive layer is an amorphous silicon layer, a polycrystalline silicon layer or a composite layer thereof.

16. (Currently amended) The method of Claim 14 wherein the reaction-preventing nitride layer is a silicon nitride layer.

17. (Original) The method of Claim 16 wherein the silicon nitride layer is formed by a plasma nitration method at a temperature of about 600°C or less.

18. (Original) The method of Claim 16 wherein the silicon nitride layer is formed by a chemical vapor deposition method at a temperature of about 600°C or less or an atomic layer deposition method at a temperature of about 600°C or less.

19. (Original) The method of Claim 16 wherein the silicon nitride layer is formed by a microwave-type deposition method at a temperature of about 600°C or less.

20. (Original) The method of Claim 14, wherein the dielectric layer is a metal oxide layer.
21. (Original) The method of Claim 20 wherein the metal oxide layer is at least one selected from the group consisting of a TiO<sub>2</sub> layer, an Al<sub>2</sub>O<sub>3</sub> layer, an Y<sub>2</sub>O<sub>3</sub> layer, a ZrO<sub>2</sub> layer, an HfO<sub>2</sub> layer, a BaTiO<sub>3</sub> layer, an SrTiO<sub>3</sub> layer and a composite layer thereof.
22. (Original) The method of Claim 20 wherein the metal oxide layer is formed by a chemical vapor deposition method at a temperature of about 600°C or less or by an atomic layer deposition method at a temperature of about 600°C or less.
23. (Original) The method of Claim 14 wherein the second conductive layer is an amorphous silicon layer, a polycrystalline silicon layer, a Ru layer, a Pt layer, an Ir layer, a TiN layer, a TaN layer, a WN layer and a composite layer thereof.
24. (Currently amended) A method of forming a capacitor comprising:  
forming an insulation layer pattern having a contact hole on a substrate having a lower structure;  
forming a first conductive layer continuously on a sidewall portion and a bottom portion of the contact hole and on the surface of the insulation layer pattern;  
removing the first conductive layer formed on the surface portion of the insulation layer pattern;  
removing the insulation layer pattern to allow the first conductive layer to remain on the sidewall portion and the bottom portion of the contact hole to form a cylindrical lower electrode;  
forming a reaction-preventing nitride layer on the cylindrical lower electrode for preventing an oxidation at a temperature of not generating a phase change of the lower electrode;

forming a dielectric layer on the reaction preventing nitride layer; and  
forming a second conductive layer on the dielectric layer as an upper electrode.

25. (Previously presented) The method of Claim 24 wherein the first conductive layer is an amorphous silicon layer, a polycrystalline silicon layer or a composite layer thereof.

26. (Previously Presented) The method of Claim 24 wherein the reaction preventing layer is formed by a plasma nitration method at a temperature of about 600°C or less, a chemical vapor deposition method at a temperature of about 600°C or less or an atomic layer deposition method at a temperature of about 600°C or less.

27. (Previously Presented) The method of Claim 24 wherein the dielectric layer is at least one selected from the group consisting of a TiO<sub>2</sub> layer, an Al<sub>2</sub>O<sub>3</sub> layer, a Y<sub>2</sub>O<sub>3</sub> layer, a ZrO<sub>2</sub> layer, an HfO<sub>2</sub> layer, a BaTiO<sub>3</sub> layer, an SrTiO<sub>3</sub> layer and a composite layer thereof.

28. (Original) The method of Claim 24 wherein the dielectric layer is formed by a chemical vapor deposition method at a temperature of about 600°C or less or by an atomic layer deposition method at a temperature of about 600°C or less.

29. (Original) The method of Claim 24 wherein the second conductive layer is one of an amorphous silicon layer, a polycrystalline silicon layer, an Ru layer, a Pt layer, an Ir layer, a TiN layer, a TaN layer, a WN layer and a composite layer thereof.

30. (Original) The method of Claim 24 wherein the lower structure includes a contact plug connected to the lower electrode.

31. (New) The method of Claim 1 wherein the nitride protection layer comprises an electrically non-conductive layer.

32. (New) A method of forming a capacitor on an integrated circuit comprising:  
forming a lower electrode of the capacitor on an integrated circuit substrate;  
forming an electrically non-conductive protection layer on the lower electrode at a  
temperature below a minimum temperature associated with a phase change of the lower  
electrode;  
forming a dielectric layer on the protection layer, wherein the protection layer is  
configured to limit oxidation of the lower electrode during forming of the dielectric layer; and  
forming an upper electrode of the capacitor on the dielectric layer.